

**ABSTRACT**

A method is provided for erasing a nonvolatile memory cell that includes a source region, a drain region, a floating gate electrode and a control gate electrode to which an erase signal is applied. In accordance with the method, a source bias voltage is applied to the source region, a drain bias voltage is applied to the drain region, and a frequency/time domain based voltage signal is applied to the control gate electrode of the cell as the erase signal.